



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Warren M. Farnworth

Serial No.: 10/672,098

Filed: September 26, 2003

For: APPARATUS AND METHODS FOR
USE IN STEREOLITHOGRAPHIC
PROCESSING OF COMPONENTS AND
ASSEMBLIES

Examiner: Unknown

Group Art Unit: Unknown

Attorney Docket No.: 2269-3996.2US
(99-0254.02/US)

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In compliance with the duty to disclose information material to patentability pursuant to 37 C.F.R. § 1.56, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the documents listed on attached Form PTO-1449 or PTO/SB/08 be considered by the Examiner and made of record. Copies of the listed documents are enclosed pursuant to 37 C.F.R. § 1.98(a).

In accordance with 37 C.F.R. § 1.97(g) and (h), filing of this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made or an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b). Further, no representation is made by Applicant herein that no other possible material information as defined in 37 C.F.R. § 1.56 (b) exists.

U.S. Patent Documents

<u>U.S. Patent No.</u>	<u>Publication Date</u>	<u>Patentee</u>
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6,259,962	07/10/01	Gothait
6,268,584	07/31/01	Keicher et al.
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6,337,122	01/08/02	Grigg et al.
6,391,251	05/21/02	Keicher et al.
6,432,752	08/13/02	Farnworth
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6,593,171	07/15/03	Farnworth
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Other Documents

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U.S. Patent Application No. 09/589,841, filed June 8, 2000, entitled "Stereolithographic Methods for Forming a Protective Layer on a Semiconductor Device Substrate and Substrates Including Protective Layers So Formed", inventor Farnworth et al.

U.S. Patent Application No. 09/590,646, filed June 8, 2000, entitled "Reinforced, Self-Aligning Conductive Structures for Semiconductor Device Components and Methods for Fabricating Same", inventor Williams et al.

U.S. Patent Application No. 09/651,930, filed August 31, 2000, entitled "Semiconductor Device Including Leads in Communication with Contact Pads Thereof and a Stereolithographically Fabricated Package Substantially Encapsulating the Leads and Methods for Fabricating the Same", inventor Salman Akram

U.S. Patent Application No. 10/191,424, filed July 8, 2002, entitled "Semiconductor Devices with Permanent Polymer Stencil and Method for Manufacturing the Same", inventor Farnworth et al.

U.S. Patent Application No. 10/201,208, filed July 22, 2002, entitled "Thick Solder Mask for Confining Encapsulant Material Over Selected Locations of a Substrate, Assemblies Including the Solder Mask, and Methods", inventor Grigg et al.

U.S. Patent Application 10/370,755, filed February 20, 2003, entitled "Chip Scale Package Structures and Method of Forming Conductive Bumps Thereon", inventor Warren M. Farnworth

U.S. Patent Application No. 10/608,749, filed June 26, 2003, entitled "Methods for Labeling Semiconductor Device Components", inventor Grigg et al.

U.S. Patent Application No. 10/619,918, filed July 15, 2003, entitled "Stereolithographic Methods for Fabricating Hermetic Semiconductor Device Packages and Semiconductor Devices Including Stereolithographically Fabricated Hermetic Packages", inventor Warren M. Farnworth

U.S. Patent Application No. 10/642,908, filed August 18, 2003, entitled "Solder Masks for Use on Carrier Substrates, Carrier Substrates and Semiconductor Device Assemblies Including Such Solder Masks, and Methods", inventor Tan et al.

U.S. Patent Application No. 10/663,402, filed September 16, 2003, entitled "Processes for Facilitating Removal of Stereolithographically Fabricated Objects from Platens of Stereolithographic Fabrication Equipment, Object Release Elements for Effecting Such Processes, Systems and Fabrication Processes Employing the Object Release Elements, and Objects Which Have Been Fabricated Using the Object Release Elements", inventor Farnworth et al.

U.S. Patent Application No. 10/688,354, filed October 17, 2003, entitled "Thick Solder Mask for Confining Encapsulant Material Over Selected Locations of a Substrate and Assemblies Including the Solder Mask", inventor Grigg et al.

U.S. Patent Application No. 10/690,417, filed October 20, 2003, entitled "Methods of Coating and Singulating Wafers and Chip-Scale Packages Formed Therefrom", inventor Farnworth et al.

Applicant offers to supply any explanation or discussion of the documents which the Examiner feels is necessary or desirable and which is requested.



Serial No. 10/672,098

This Supplemental Information Disclosure Statement is filed before the mailing date of the first Office Action on the merits and no fee is due.

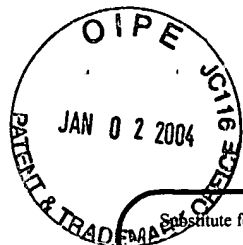
Respectfully submitted,

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Date: December 30, 2003
TLW/sls:rmh

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STATEMENT BY APPLICANT**

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Sheet 1 of 6

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Filing Date	September 26, 2003
First Named Inventor	Warren M. Farnworth
Group Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	3996.2US (99-0254.02/US)

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
		US-6,251,488	06/26/01	Miller et al.	
		US- 6,259,962	07/10/01	Gothait	
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		US- 6,432,752	08/13/02	Farnworth	
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		US-6,607,689	08/19/03	Farnworth	
		US-6,635,333	10/21/03	Grigg et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
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2

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Application Number	10/672,098
Filing Date	September 26, 2003
First Named Inventor	Warren M. Farnworth
Group Art Unit	Unknown
Examiner Name	Unknown
Attorney Docket Number	3996 211S (99-0254 02/11S)

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

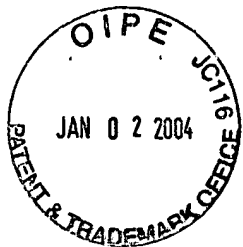
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		U.S. Patent Application Publication 2002/0066966 A1 to Farnworth, dated June 6, 2002	
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		U.S. Patent Application Publication 2003/0068584 A1 to Farnworth et al., dated April 10, 2003	
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		Application Number	10/672,098
		Filing Date	September 26, 2003
		First Named Inventor	Warren M. Farnworth
		Group Art Unit	Unknown
		Examiner Name	Unknown
		Attorney Docket Number	3996 211S (99-0254 02/11S)

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
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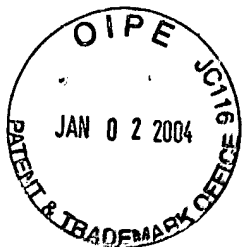
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5

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		U.S. Patent Application No. 09/589,841, filed June 8, 2000, entitled "Stereolithographic Methods for Forming a Protective Layer on a Semiconductor Device Substrate and Substrates Including Protective Layers So Formed", inventor Farnworth et al.	
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Attorney Docket Number	3996 211S (99-0254 02/11S)

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		U.S. Patent Application No. 10/663,402, filed September 16, 2003, entitled "Processes for Facilitating Removal of Stereolithographically Fabricated Objects from Platens of Stereolithographic Fabrication Equipment, Object Release Elements for Effecting Such Processes, Systems and Fabrication Processes Employing the Object Release Elements, and Objects Which Have Been Fabricated Using the Object Release Elements", inventor Farnworth et al.	
		U.S. Patent Application No. 10/688,354, filed October 17, 2003, entitled "Thick Solder Mask for Confining Encapsulant Material Over Selected Locations of a Substrate and Assemblies Including the Solder Mask", inventor Grigg et al.	
		U.S. Patent Application No. 10/690,417, filed October 20, 2003, entitled "Methods of Coating and Singulating Wafers and Chip-Scale Packages Formed Therefrom", inventor Farnworth et al.	

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